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APPLICATION FOR LETTERS PATENT

for

METAL STRUCTURES FOR INTEGRATED CIRCUITS AND METHODS FOR MAKING THE SAME

Inventors:

Mike Vyvoda
Steve Radigan
K. Leo Zhang

METAL STRUCTURES FOR INTEGRATED CIRCUITS AND METHODS FOR MAKING THE SAME

[01] FIELD OF THE INVENTION

[02] The invention generally relates to methods for fabricating integrated circuits (ICs) and semiconductor devices and the resulting structures. More particularly, the invention relates to metal structures used in ICs and methods for making such structures. Even more particularly, the invention relates to IC metal structures protected from and resistant to peeling and methods for making such structures.

[03] BACKGROUND OF THE INVENTION

[04] In IC fabrication, metal structures and metal layers are used extensively as conducting paths in the circuit. Indeed, multiple levels of metal layers (above an underlying substrate) are typically employed when manufacturing the IC. The multiple metal layers are employed in order to accommodate higher densities, allowing device dimensions to shrink well below one micron. Thus, ICs having three and four levels (and more) of metallization are becoming more prevalent as device geometries shrink to sub-micron levels.

[05] One common metal used for forming such metal layers (also referred to as metal lines or metal wiring) is Tungsten (W). Tungsten is also used as a material for forming interconnections in vias to connect the different metal layers. The size (e.g., width) of the

tungsten structures typically ranges from "large" structures (with the smallest dimension greater than about 1 microns) to "small" structures (with the smallest dimension less than about 0.25 microns). As the size of ICs decrease, even smaller metal structures will necessarily be used.

[06] As with other IC fabrication methods, devices containing metal structures are often subjected to heat treatments. Such heat treatments can often cause problems with the metal structures. See, for example, U.S. Patent No. 6,184,118, the disclosure of which is incorporated herein by reference. In particular, tungsten structures can often "peel" during heat treatments and especially during aggressive heat treatments, e.g., those lasting for about 1 minute at a temperature of about 800°C. When the tungsten structures delaminate or peel, they can cause electrical failure in that wafer die where the peeling occurs. As well, such peeling can also cause high defect densities in adjacent dies on the wafer since the peeled metal can move to adjacent dies. Finally, such peeling can contaminate fabrication equipment, resulting in widespread defect problems.

[07] To overcome this problem, many manufacturers employ very strict topological design requirements, even if they do not use aggressive heat treatments. For example, some manufacturers will not make tungsten structures with dimensions greater than 1 micron because of the problems noted above. Without larger tungsten structures, many IC devices can be limited in their features and functionality. For example, slotting or waffling techniques are often used to meet maximum size requirements while providing

wider (lower resistance) metal lines. Such techniques, however, can make the total size of high-current-carrying structures, such as bus lines, larger than if no slotting was needed. Also, it is often difficult to use such techniques within areas of the wafer having irregular circuit features.

[08] SUMMARY OF THE INVENTION

[09] The present invention provides metal structures for ICs and methods for manufacturing the same. The metal structures range from small features to large features and withstand peeling problems during heat treatments that occur during the manufacturing process. The invention is able to reduce or prevent peeling of the metal structures from the underlying structures or substrates. The peeling problems are reduced or prevented by including a capping layer or capping structure over the dielectric layer over the metal structure and then annealing the capping layer or capping structure, thereby enhancing the adhesion of the metal structure to the underlying structure or substrate.

[10] BRIEF DESCRIPTION OF THE DRAWINGS

[11] Figures 1-5, 6a, 6b, 6c, 6d, and 7 are views of one aspect of the IC metal structures and methods of making the same according to the invention, in which:

[12] Figures 1 and 2 illustrate various substrates on which the metal structures of the invention can be formed;

[13] Figures 3-5 illustrate the sequence of steps in one aspect of process of the invention;

[14] Figures 6a, 6b, 6c, and 6d illustrate the various configurations of the capping structure of the invention; and

[15] Figure 7 illustrates the sequence of steps in one aspect of process of the invention;

[16] Figures 1-5, 6a, 6b, 6c, 6d, and 7 presented in conjunction with this description are views of only particular—rather than complete—portions of the IC metal structures and methods of making the same according to the invention.

[17] DETAILED DESCRIPTION OF THE INVENTION

[18] The following description provides specific details in order to provide a thorough understanding of the present invention. The skilled artisan, however, would understand that the present invention can be practiced without employing these specific details. Indeed, the present invention can be practiced by modifying the illustrated structure and method, and can be used in conjunction with apparatus and techniques conventionally used in the industry. For example, while the invention is described with reference to IC devices, it could be modified for other devices that require metal structures such as MEMS devices. As well, the invention is described with reference to tungsten metal structures, but could be used for other refractory metals (and their alloys) like cobalt,

refractory metal silicides such as $TiSi_2$, or other non-refractory metals (or their alloys) like aluminum, as well as other metals that delaminate under heat treatments.

[19] As illustrated in Figure 1, the process of the invention begins with a substrate. The substrate can be any suitable substrate (or surface) known in the art on which a metal structure can be formed. Example of such substrates include a metal structure like a metal interconnect in a via, a pre-formed portion (or section) of an IC device like a CMOS substrate, or a dielectric layer. In a preferred aspect of the invention, a CMOS substrate 102 (similar to that illustrated in Figure 1) is employed as the substrate used in the invention. CMOS substrate 102 contains those portions of an IC device which, when combined with the overlying metallization as well as additional components, will form a CMOS device. Examples of such components (as illustrated in Figure 1) include: wafer 10; field oxide regions 12, 14, and 16; gate regions 24 and 26 containing gates 30 and 32, gate oxides 20 and 22, sidewall spacers 42, 44, 46, and 48; source regions 52 and 56; drain regions 54 and 58; and source-drain extension regions 38 and 40.

[20] As shown in Figure 2, a dielectric layer 104 can be deposited over the entire CMOS substrate 102. The dielectric layer 104 operates to insulate CMOS substrate 102 from the overlying features that will be subsequently formed. After deposition, dielectric layer 104 can be substantially planarized using any planarization process known in the art, e.g., chemical-mechanical polishing (CMP). In some aspects of the invention this planarization step is not needed.

[21] At this stage, if desired, a capping structure similar to that described below can be formed. Usually, a capping structure is not needed at this location in most aspects of the invention and so is described in detail below.

[22] After providing the substrate, a first metallization layer 106 is formed as illustrated in Figure 3. For metallization layer 106 to contact CMOS substrate 102, a contact 108 is first formed before forming the first metallization layer. As known in the art, contact 108 is formed through the dielectric layer 104 overlying CMOS substrate 102. The contact is formed using standard processing techniques known in the art by depositing a photoresist layer, developing the photoresist layer to expose an upper surface of the dielectric layer above the desired region of contact 108, etching the dielectric layer using the developed photoresist layer and, for example, a C_3F_8 and CO plasma etchant, and then stripping the photoresist layer with an O_2 plasma, followed by a wet chemical strip.

[23] The first metallization layer 106 is then deposited. The first metallization layer can comprise any metal, metal alloys, or metal compounds (or combinations thereof) known in the art that—whether alone or combined—function as a metallization layer. Examples of such metals include tungsten, titanium, aluminum, copper, and refractory metals other than tungsten, as well as their alloys and compounds. The thickness of the metallization layer (or respective thicknesses of individual layers making up the

metallization layer) can be any thickness known in the art that provides the desired physical and electrical characteristics needed for the metallization layer.

[24] In a preferred aspect of the invention, as illustrated in Figure 4, the first metallization layer 106 includes a combination of several layers. The first layer is a titanium (Ti) layer 110 with a thickness of about 150 Å. The second layer is a titanium nitride (TiN) layer 112 with a thickness of about 100 Å. The third layer is a W layer 114 with a thickness of about 3000 Å. The fourth and final layer of the first metallization layer 106 is a TiN layer 116 with a thickness of about 250 Å. These various layers can be deposited using any known technique in the art providing the necessary physical characteristics, such as the ability to fill contact holes 108. Examples of such known techniques include sputtering or chemical vapor deposition (CVD). As well, for the upper TiN layer, a titanium layer could be deposited and then nitrided in a nitrogen-containing atmosphere as known in the art.

[25] Next, first metallization layer 106 is patterned to obtain the desired metal lines. Any suitable process patterning the metallization layer 106 into the metal lines can be employed in the invention. For example, one standard processing technique known in the art that can be used deposits a photoresist layer over the metallization layer, develops the photoresist layer to expose an upper surface of the metallization layer 106 to be removed, etches the metallization layer using the developed photoresist layer and, for example, a

SF_6 and N_2 plasma etchant, and then strips the photoresist layer using a NF_3 and O_2 plasma, followed by a wet chemical strip.

[26] Next, as illustrated in Figure 5, a first dielectric layer 120 (or combination of dielectric layers) is deposited over the metal lines formed from metallization layer 106. Any dielectric material known in the art can be used in first dielectric layer of the invention. Examples of dielectric materials include silicon nitride (Si_xN_y), silicon oxide (SiO_2), and low-k dielectrics such as fluorinated SiO_2. The thickness of the first dielectric layer 120 is any suitable thickness that will provide the desired electrical insulation characteristics. In one aspect of the invention, a high-density plasma CVD (HDP-CVD) silicon oxide layer is deposited to a thickness of about 9000 Å. The first dielectric layer 120 is then substantially planarized using any suitable process, such as CMP. In one aspect of the invention, the planarization process reduces the thickness for the HDPCVD silicon oxide layer to about 3000 Å above the upper surface of the patterned metallization layer.

[27] After planarizing the first dielectric layer 120, a first capping structure ("first cap") is deposited over the first dielectric layer. The first cap operates to reduce or eliminate the peeling between the first metallization layer and its underlying substrate (i.e., first dielectric layer) that can occur when the first metallization layer is subjected to heat treatments.

[28] The first cap can be configured with any shape or size that will obtain the desired function. In one aspect of the invention, the first cap can be a continuous or substantially continuous layer(s) as illustrated in Figure 6a. In another aspect of the invention, the first cap is not continuous, e.g., it may be substantially contiguous at discrete points as illustrated in Figure 6b. Another example of the non-continuous first cap is illustrated in Figures 6c and 6d, where the first cap may have sections with a material and sections without a material. Non-continuous caps are not preferred in the invention because of the additional processing (and costs) required to make a non-continuous layer.

[29] Any material that operates as a cap as described above between the underlying substrate and the overlying metallization layer can be used in first cap of the invention. Examples of cap materials include non-conducting materials—like highly-resistive semiconductor materials such as undoped amorphous Si—and dielectric materials like phosphosilicate glass (PSG), plasma-enhanced CVD (PECVD) silane oxide, PECVD TEOS oxide, APCVD or LPCVD TEOS or PSG, HDP-CVD SiO_2, and BPSG. In one aspect of the invention, several layers can be combined to operate as the first cap. The thickness of the cap material (or materials) need only be sufficient to provide the desired function. Generally, the thickness of the first cap can range from about 250 Å to about 10,000 Å.

[30] In one aspect of the invention, when the first metallization layer described above is used, the first cap employed is made of the material described below and made in the

following manner. First, as illustrated in Figure 5, a PSG layer 122 is deposited to a thickness of about 2000 Å using any known technique in the art, e.g., atmospheric-pressure CVD (APCVD). The PSG layer is then annealed at a temperature and time sufficient to enhance the adhesion of the underlying metallization layer to its substrate (i.e., the first dielectric layer under the first metallization layer). In one aspect of the invention, the PSG layer is annealed for about 30 minutes in an inert or non-reactive atmosphere (e.g., nitrogen or helium) at a temperature of about 700°C. In another aspect of the invention, the annealing process can be performed in a similar atmosphere for about 60 minutes at a temperature of about 675°C. Similar temperatures, times, and atmospheres which accomplish this annealing function can be employed in the invention. For example, a rapid thermal annealing (RTA) treatment at 700°C for 60 seconds in an argon ambient could be used. Other temperature and time combinations for RTA treatments can be used in this aspect of the invention.

[31] Next, as illustrated in Figure 7, via 124 is formed in the first cap (when present) and first dielectric layer 120. The via 124 can be formed using standard processing techniques known in the art, e.g., depositing a photoresist layer, developing the photoresist layer to expose an upper surface of the desired region of via 124, etching the first cap (when present), and the first dielectric layer using the developed photoresist layer and, for example, a C_3F_8 and CO plasma etchant, and then stripping the photoresist layer using an O_2 plasma followed by a wet chemical strip.

[32] Then, the second metallization layer 126 is deposited as illustrated in Figure 7. The second metallization layer 126 can comprise any metal, metal alloys, or metal compounds (or combinations thereof) known in the art that—whether alone or combined—function as a metallization layer. Examples of such metals include tungsten, titanium, aluminum, copper, and their alloys and compounds. The thickness of the second metallization layer (or respective thicknesses of individual layers making up the metallization layer) can be any thickness known in the art that provides the desired characteristics needed for the metallization layer.

[33] In a preferred aspect of the invention, the second metallization layer 126 includes a combination of several layers substantially similar to the first metallization layer. Thus, as illustrated in Figure 4, the second metallization layer 126 contains a first titanium (Ti) layer 110 with a thickness of about 150 Å. The second layer is a titanium nitride (TiN) layer 112 with a thickness of about 100 Å. The third layer is a W layer 114 with a thickness of about 3000 Å. The fourth and final layer of the first metallization layer 106 is a TiN layer 116 with a thickness of about 250 Å. These various layers can be deposited using any known technique in the art as described above, such as sputtering or chemical vapor deposition (CVD). As well, for the upper TiN layer, a titanium layer could be deposited and then nitrided in a nitrogen-containing atmosphere as known in the art.

[34] Then, second metallization layer 126 is patterned to obtain the desired metal lines. Any suitable process patterning the metallization layer into the metal lines can be

employed in the invention. For example, one standard processing technique known in the art that can be used deposits a photoresist layer over the metallization layer, develops the photoresist layer to expose an upper surface of the metallization layer to be removed, etches the metallization layer using the developed photoresist layer and a SF_6 and N_2 plasma etchant, and then strips the photoresist layer using an NF_3 and O_2 plasma followed by a wet chemical strip.

[35] Next, a second dielectric layer 130 (or combination of dielectric layers) is deposited over the metal lines formed from second metallization layer 126. Any dielectric material known in the art can be used in second dielectric layer of the invention. Examples of dielectric materials include silicon nitride (SiNx), silicon oxides (SiO_2), and low-k dielectrics such as fluorinated SiO2. The thickness of the second dielectric layer is any suitable thickness that will provide the desired electrical insulation characteristics. In one aspect of the invention, a high-density plasma CVD (HDP-CVD) silicon oxide layer is deposited to a thickness of about 9000 Å. The second dielectric layer is then substantially planarized using any suitable process, such as CMP. In one aspect of the invention, the planarization process reduces the thickness, e.g., for the HDPCVD silicon oxide layer the thickness can be decreased to about 3000 Å above the top of the second dielectric layer.

[36] In one aspect of the invention, a second capping structure ("second cap") can be deposited over the second dielectric layer. The second cap 132 serves a similar function,

can be made of a similar material, can be formed in similar configuration(s), and can be formed in a similar manner as the first cap. When used, the second cap is then followed by another annealing process similar to the annealing process used for the first cap.

[37] Generally, the invention is able to reduce or prevent peeling of metallization layer or metal structure "n" from an adjacent (usually underlying) layer or structure. To obtain that result, a capping layer or capping structure is deposited over the inter-metal dielectric layer overlying the metal layer or metal structure. Then, an annealing step is performed—it is believed—to "pin down" the underlying metal layer/structure by enhancing the adhesion of the metal layer/structure to the underlying layer or structure.

[38] After the above processes are concluded, conventional processing can continue to finish the IC device. For example, additional metallization (including underlying and overlying caps) and additional dielectric layers can be formed. As well, the other components to complete the CMOS device can be formed.

[39] Having described the preferred embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.